

A Low-Power Architecture for Integrating Analog-to-Digital Converters

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Abstract— This paper reports on a modified architecture for single-slope integrating analog-to-digital converter (ADC) for use in image sensors and biomedical or any other applications where the value of the input analog signal has small and slow variations. In this architecture, instead of digitizing every new analog sample independently, the difference of the new sample with the previous sample is digitized. This idea will therefore considerably reduce the power consumption of the ADC. In order to illustrate the effectiveness of the proposed idea, an 8-bit, 4 kS/s ADC is designed and simulated in a 0.18 μ m CMOS technology. The proposed ADC is very power efficient when the input signal is very slow and has a small variation in voltage amplitude. Simulations confirm that the proposed ADC architecture shows more than 80% power saving compared to conventional architecture for an input signal amplitude of 0.2 V_{FS} .

I. INTRODUCTION

Integrating analog-to-digital converters (ADCs) are commonly used for high-accuracy yet low-speed applications [1, 2]. These converters have very small offset and gain errors and are highly linear. Another advantage of integrating A/D converters is the small amount of circuitry required in their implementation that makes them suitable for ultra-low-power applications. Biomedical signals are often very slow (<1 kHz) and have limited dynamic range. But, power consumption and area are important considerations for these applications.

Also, for many biomedical signals as well as the image information, the difference between two successive samples is much smaller than the full-scale voltage. Therefore, digitizing the difference signal instead of each new sample independently can lead to considerable power saving. In this paper, a novel architecture for integrating ADC based on the idea is proposed. In this architecture, if the input signal changes very slowly, that is the case for many biomedical signals or image information in individual pixels of image sensors, the ADC will work for a short time interval proportional to the difference between successive values and will go to power-down mode for the rest of the time. In this time, the comparator and the counter are switched off and only the output latches and the digital circuit consumes the power. The rest of the paper is organized as follows. Section II introduces the conventional integrating ADC and explains the dual-slope and single-slope architectures currently used in these ADCs. Section III explains the architecture of the

proposed ADC. Circuit design considerations are discussed in Section IV. Simulation results of the ADC and a discussion on the effectiveness of the proposed architecture are addressed in Section V followed by conclusions in Section VI.

II. BACKGROUND

Integrating ADCs are mainly divided in two types of dual-slope and single-slope ADCs. In this section we introduce these two types of ADCs.

A. Single-Slope ADC

A simple structure for an integrating ADC, reported in [2], is an implementation example for a single-slope ADC shown in Fig. 1. In this structure a current reference, I_0 is used instead of a voltage reference. So the slope of discharging the capacitor is proportional to I_0 . The circuit works as follows. During $\Phi 1$, S1 and S3 are closed, and the input voltage, V_{in} , is stored in C_{INT} . During $\Phi 2$, S4 and S5 are closed to shift the voltage of C_{INT} by V_{ref} . During $\Phi 3$, S2, S4, and S5 are closed to discharge C_{INT} by the constant current of I_{ref} , meanwhile, the counter measures the time for C_{INT} to be discharged back to V_{ref} [2].

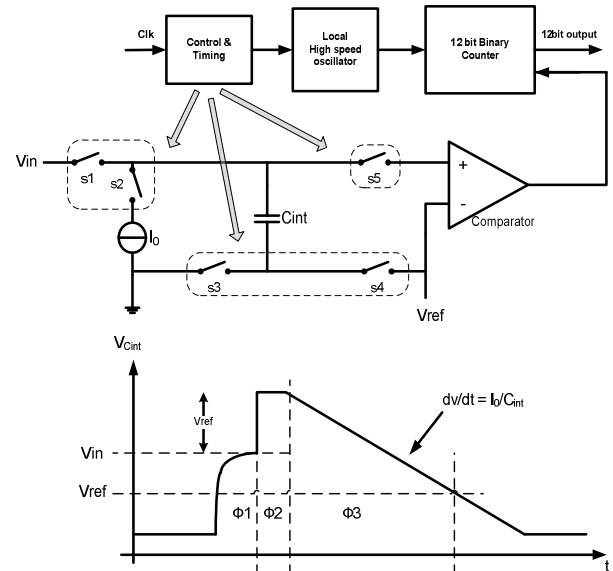


Fig. 1 Block diagram and timing diagram example for a single-slope integrating ADC [2]

B. Dual Slope ADC

The conventional structure mostly used in the high resolution ADCs, is dual-slope ADC that compared to single-slope ADC has less sensitivity to the offset and the time constant of the integrator. A simplified diagram for a dual-slope integrating converter is shown in Fig 2 [1].

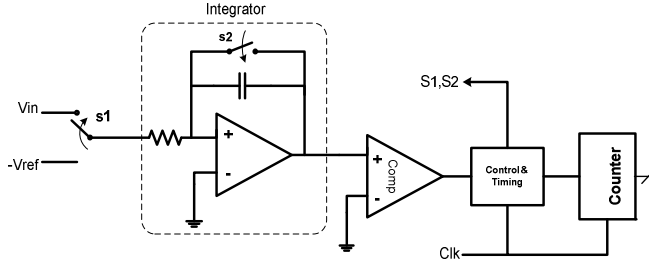


Fig. 2 implementation of Dual-slope ADC [1]

Conventionally, in both types of integrating ADCs, each new sample is considered independently regardless of the value of the previous sample. This fact reduces the power efficiency of the ADC. Also, after the comparison, the comparator is not required until the next sampling period. So we can turn off the comparator during this time. In the following section, we propose a modified implementation for a single-slope integrating ADC based on digitizing the difference between two successive samples, instead of digitizing each sample independently.

III. THE PROPOSED LOW-POWER A/D CONVERSION

In many applications, most of the time, the difference between the values of two successive samples of the analog signal is small compared to the signal full-scale range. From power-consumption viewpoint, it thus seems advantageous to digitize the difference of the new sample with the previous sample instead of digitizing every new sample independently. Specifically, in an image sensor, the difference between the intensity of light (and thus the corresponding voltage of a pixel) between two adjacent pixels is much smaller than the full-scale range. In time domain, also, the difference of the light intensity of two successive frames is usually much smaller than the full-scale range for the majority of the pixels. Therefore, if an individual ADC in addition to a multiplexer are used in the image sensor, digitizing the differences of the pixels' voltages instead of each pixel seems reasonable.

In the integrating ADC, the power is mainly consumed in the counter, the operational amplifier of the integrator and the comparator. Therefore, if these blocks are functioning just for digitizing the differences of successive samples which takes much less time than each new sample independently, and are turned off during the rest of the time, considerable power will be saved.

Therefore, instead of conventional A/D conversion, we can store the output of each conversion and only measure the difference between each new sample with the stored value. Hence, the counting time of the counter in every conversion is

reduced and the counter as well as the comparator can be turned off until the next sample is being sampled (in a synchronous sampling). This idea can save a great amount of power in applications in which the input voltage changes are not very fast and large.

Fig. 3 compares the timing diagrams of the conventional and the proposed integrating ADCs. As can be observed for the given example, the circuit in the proposed architecture is idle for most of the time and thus the power consumption is much lower; nevertheless, the power consumption is proportional to signal activity.

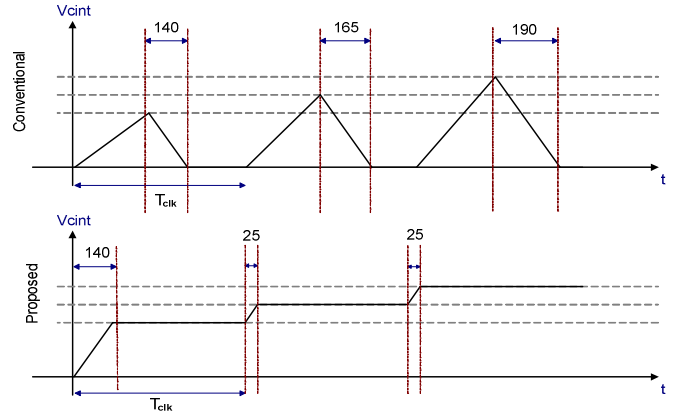


Fig. 3 Comparison of timing diagrams for the conventional and the proposed architecture

For implementing the idea, the architecture reported in [2] has been modified as shown in Fig. 4. A current source is used to charge (or discharge) the integrating capacitor, C_{INT} , to the value of the input sample. For each new sample, if the value of this sample, V_{new} , is higher than the value of the previous sample, V_{old} , S0 is connected and I_{ref} charges the capacitor and the counter counts up until it is stopped by the comparator. If V_{new} is lower than V_{old} , S1 and S2 are connected and the mirrored current of I_{ref} discharges the capacitor and the counter counts down until the comparator stops it at the new value. As soon as the comparator stops the counter, both the counter and the comparator will go to the power-down mode thus considerable power is saved.

IV. IMPLEMENTATION OF THE ADC

In this section, practical implementation considerations of an ADC with the proposed architecture are addressed. The

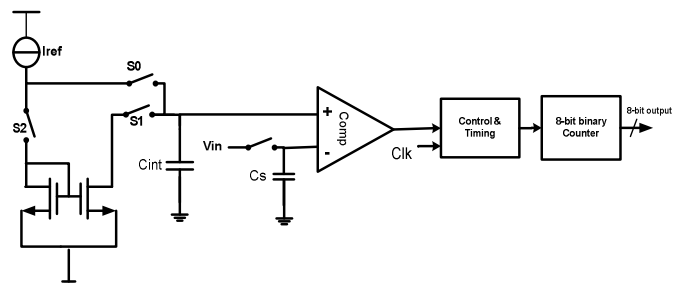


Fig. 4 The block diagram for the proposed architecture

proposed ADC includes a reference current, I_{ref} , the comparator and the counter. The maximum time required between two consecutive samples, T_{max} , equals

$$T_{max} = T_s = \frac{1}{f_s} = \frac{C_{INT} \times V_{FS}}{I_{ref}} = 2^N T_{clk} \quad (1)$$

where T_s and f_s are the sampling period and frequency, respectively. Here, required specifications for the current source and the comparator are first discussed and then the sources of error are investigated.

A. Current Source

For a non-ideal current source where the output impedance is finite, the value of the current will be dependant on the output voltage therefore introducing a non-linearity to the entire ADC. In order to reduce this non-linearity below the accepted level imposed by the ADC resolution, the output impedance must be high enough.

The implementation of the current mirror circuit is illustrated in Fig 5 [3]. The employed cascode structure provides a large enough output resistance while the minimum headroom voltage is $2V_{DS-sat}$ that is suitable for our design. The mirror circuit is similar to this circuit except for using PMOS transistors instead of NMOS one.

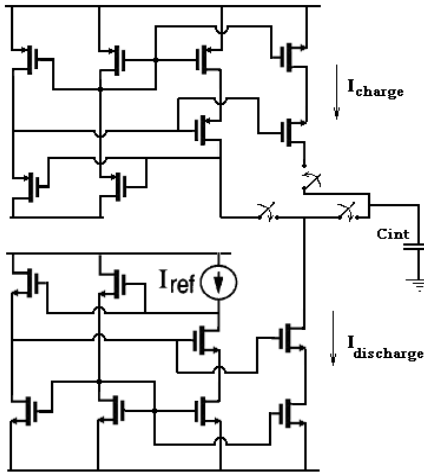


Fig. 5 reference Current circuit

B. Comparator

The most important part of this ADC is its comparator because, not only the comparator resolution must be smaller than the ADC resolution, but also a reasonable speed is needed to have a minimum delay in the comparator. Note that D_{out} is proportional to the time measured by the counter beginning from the sampling instance until the comparator output changes. So the delay of the comparator influences on the measured time.

Another consideration in the comparator design is the fact that the input common-mode voltage of the comparator varies

for different levels of the input sample. In order for the comparator to be fully functional with acceptable performance for the entire input common-mode range, the architecture proposed in [4] has been modified to the circuit configuration depicted in Fig. 6.

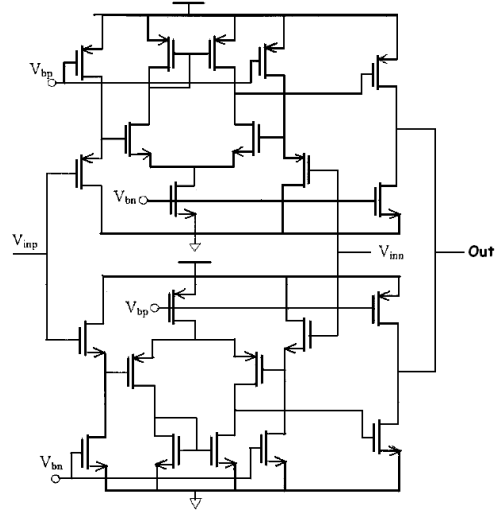


Fig. 6 Rail to Rail comparator

C. Error Sources

The most important design concern in the proposed architecture is the accumulation of errors from one sample to another. The main error sources in this ADC are the finite output resistance of the current source, the time error of the counter and the comparator offset and delay.

For the current source, regarding the value of V_{LSB} , the current source should be designed in a way that the error due to the output resistance can be ignored compared to V_{LSB} .

$$I_{charge} = I_{ref} + I_{error} = I_{ref} + \frac{V_C}{R_{out}} \quad (2)$$

$$\Delta V_C = \frac{I_{error}}{C_{INT}} \Delta t_e, \quad \Delta V_C = \frac{V_C}{R_{out} \times C_{INT}} \Delta t_e \quad (3)$$

$$\Delta t_e = C_{INT} \left(R_{out} \times \ln \left(\frac{R_{out} I_{ref}}{R_{out} I_{ref} - V_{FS}} \right) - \frac{V_{FS}}{I_{ref}} \right) \quad (4)$$

$$\Delta t_e < T_{clk} \quad (5)$$

where Δt_e is the time error of the counter. By solving the above equation, the minimum value of R_{out} can be calculated.

The time delay between the instant when the comparator sends the stop signal and the end of the counter clock period is corresponding to an error, the second source of error in integrating ADCs. In order to insure that these timing errors are not accumulated, one can simply reset the ADC every M samples.

The third error is the offset voltage of the comparator. Here, we show that this offset voltage affects the accuracy of the ADC just for the very first sample after resetting the ADC. Assuming an offset voltage of V_{OS} for the comparator (and no other error sources in the ADC), at the beginning of second

cycle, the voltage across the integrating capacitor would be equal to $V_{in0} - V_{OS}$ and the measured time equals

$$\Delta t_0 = C_{int} \frac{(V_{in0} - V_{os})}{I_{ref}} \quad (6)$$

Now, for the following sample, the capacitor will be charged to $V_{in1} - V_{in0}$, since

$$\Delta t_1 = C_{int} \frac{(V_{in1} - V_{os} - (V_{in0} - V_{os}))}{I_{ref}} = C_{int} \frac{(V_{in1} - V_{in0})}{I_{ref}} \quad (7)$$

and similarly

$$\Delta t_N = C_{int} \frac{(V_{inN} - V_{in(N-1)})}{I_{ref}} \quad (8)$$

Therefore, we can eliminate this amount of offset by adding a calibration phase when the ADC starts.

V. SIMULATION RESULTS

We designed an 8-bit 4kS/s ADC with a full-scale voltage (V_{FS}) of 1V in a 0.18 μ m CMOS process. The ADC has been simulated using HSPICE. In this implementation, with a reference current of 0.1 μ A, the integrating capacitor has been chosen equal to 25pF. The results of simulations show that the amount of accumulated error is less than 1 LSB in every 25 samples. So we can reset the ADC in every 20 input samples to assure that the accumulated error is less than 1 LSB.

Fig 7 shows the 128 points-FFT plot of the ADC with the input frequency of $(15/128)*f_s$. The total power dissipation is 16 μ W with 0.8 V_{FS} input amplitude at Nyquist frequency. The value of signal-to-noise-and-distortion (SNDR) is 42dB. The specifications of the ADC are summarized in Table. I.

Table. II compares the power dissipation for the conventional single-slope ADC and the proposed architecture for different values of the frequency and the amplitude of the input sine wave. This Table shows that a significant reduction in power dissipation is achieved with some complexity in design. For example, for an input signal with a 0.2 V_{FS} amplitude, at least 80% power saving is observed compared to conventional architecture. This power saving increases for lower frequencies. Furthermore, despite the case for conventional implementations, the power consumption is proportional to the amplitude and frequency of the input signal.

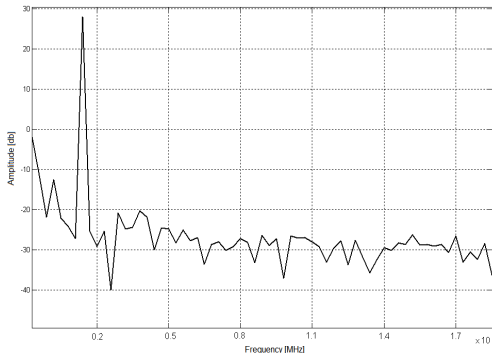


Fig. 7 FFT plot of the ADC – 128 points

Table I. Specification of ADC

Technology	Vdd	Resolution	Fs	V _{FS}	Power	THD
0.18 μ m	1.8V	8	4 kS/s	1V	16 μ W	-42 dB

Table II. Power dissipation for different frequencies and amplitudes of the input signal

	0.2 V _{FS}	0.5 V _{FS}	0.8 V _{FS}
Power Consumption (conventional, f=31/64*fs)	28.3 μ W	27.6 μ W	27 μ W
Power Consumption (Proposed, f=31/64*fs)	5.7 μ W	11.5 μ W	16 μ W
Power Consumption (Proposed, f=15/64*fs)	3.4 μ W	7.1 μ W	12.5 μ W
Power Consumption (Proposed, f=7/64*fs)	2.1 μ W	4.2 μ W	8.5 μ W

VI. CONCLUSIONS AND DISCUSSIONS

In this paper, a modified architecture was proposed for integrating A/D converters where the difference between consecutive samples is digitized instead of each new sample independently. Since, most of the ADC parts are turned off during the rest of the time, for small and slow input signals, the ADC is idle for most of the time. HSPICE simulations show that for a 0.2 V_{FS} input signal, the power of the ADC is reduced from 28 μ W for a conventional implementation to 5.7 μ W for the proposed implementation. The power saving is even more for lower-frequency sine waves or for biomedical signals.

In an image, from one image frame to the other (in the time domain), the difference between the light intensity of two successive images at a specific pixel, compared to the full-scale range, is not very large. Applying the idea explained above in digitizing the differences of samples will therefore considerably reduce the power consumption of the ADC. Besides, for most of the pixels, the difference between the intensity of light in two adjacent pixels is much smaller than the full-scale range. Thus, if a single ADC as well as a multiplexer is employed, the idea of digitizing the differences of samples seems promising for this case as well.

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