PROBLEMS

Problem B–4–1

Consider the regions in the s plane shown in Figures 4–65(a) and (b). Draw the corresponding regions in the z plane. The sampling period T is assumed to be 0.3 sec. (The sampling frequency is $\omega_s = 2\pi/T = 2\pi/0.3 = 20.9$ rad/sec.)

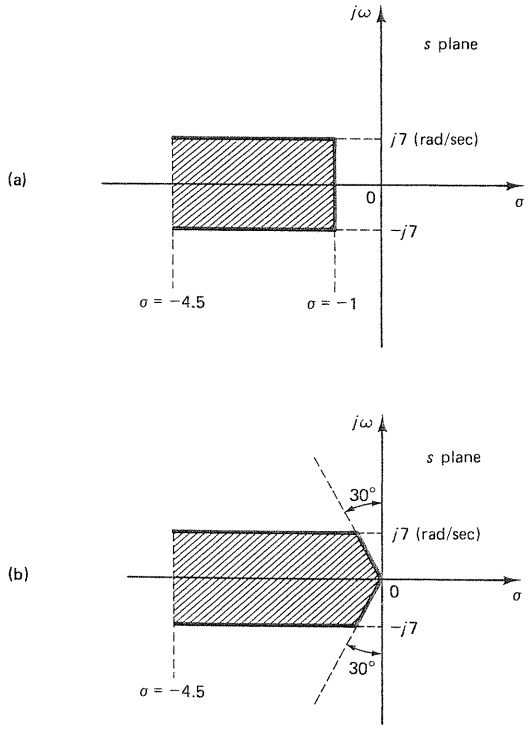

Figure 4–65 (a) Region in the s plane bounded by constant ω lines and constant σ lines; (b) region in the s plane bounded by constant ζ lines, constant ω lines, and a constant σ line.

Problem B–4–2

Consider the following characteristic equation:

$$z^3 + 2.1z^2 + 1.44z + 0.32 = 0$$

Determine whether or not any of the roots of the characteristic equation lie outside the unit circle centered at the origin of the z plane.

Problem B–4–3

Determine the stability of the following discrete-time system:

$$\frac{Y(z)}{X(z)} = \frac{z^{-3}}{1 + 0.5z^{-1} - 1.34z^{-2} + 0.24z^{-3}}$$

Problem B–4–4

Consider the discrete-time closed-loop control system shown in Figure 4–13. Determine the range of gain K for stability by use of the Jury stability criterion.

Problem B–4–5

Solve Problem B–4–4 by using the bilinear transformation coupled with the Routh stability criterion.

Problem B–4–6

Consider the system

$$\frac{Y(z)}{X(z)} = G(z) = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}}$$

Suppose that the input sequence $\{x(k)\}$ is bounded; that is,

$$|x(k)| \leq M_1 = \text{constant}, \qquad k = 0, 1, 2, \ldots$$

Show that, if all poles of $G(z)$ lie inside the unit circle in the z plane, then the output $y(k)$ is also bounded; that is,

$$|y(k)| \leq M_2 = \text{constant}, \qquad k = 0, 1, 2, \ldots$$

Problem B–4–7

State the conditions for stability, instability, and critical stability in terms of the weighting sequence $g(kT)$ of a linear time-invariant discrete-time control system.

Problem B–4–8

Consider the digital control system shown in Figure 4–66. Plot the root loci as the gain K is varied from 0 to ∞. Determine the critical value of gain K for stability. The sampling period is 0.1 sec, or $T = 0.1$. What value of gain K will yield a damping ratio ζ of the closed-loop poles equal to 0.5? With gain K set to yield $\zeta = 0.5$, determine the damped natural frequency ω_d and the number of samples per cycle of damped sinusoidal oscillation.

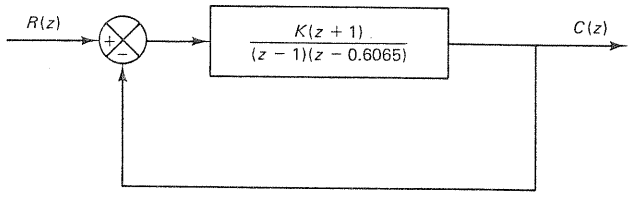

Figure 4–66 Digital control system for Problem B–4–8.

Problem B–4–9

Referring to the digital control system shown in Figure 4–67, design a digital controller $G_D(z)$ such that the damping ratio ζ of the dominant closed-loop poles is 0.5 and the number of samples per cycle of damped sinusoidal oscillation is 8. Assume that the sampling period is 0.1 sec, or $T = 0.1$. Determine the static velocity error constant. Also, determine the response of the designed system to a unit-step input.

Problem B–4–10

Consider the control system shown in Figure 4–68. Design a suitable digital controller that includes an integral control action. The design specifications are that the damping ratio ζ of the dominant closed-loop poles be 0.5 and that there be at least eight samples per cycle of damped sinusoidal oscillation. The sampling period is assumed to be 0.2

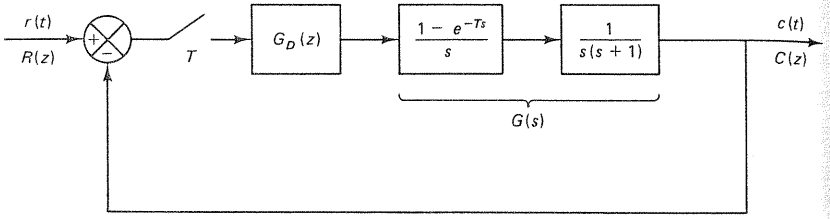

Figure 4–67 Digital control system for Problem B–4–9.

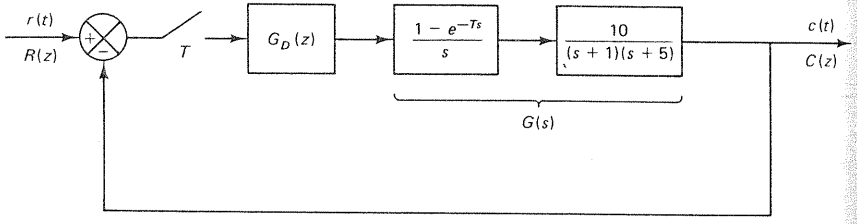

Figure 4–68 Digital control system for Problem B–4–10.

sec, or $T = 0.2$. After the digital controller is designed, determine the static velocity error constant K_v.

Problem B–4–11

Consider the digital control system shown in Figure 4–69, where the plant is of the first order and has a dead time of 5 sec. By choosing a reasonable sampling period T, design a digital PI controller such that the dominant closed-loop poles have a damping ratio ζ of 0.5 and the number of samples per cycle of damped sinusoidal oscillation is 10. After the controller is designed, determine the response of the system to a unit-step input.

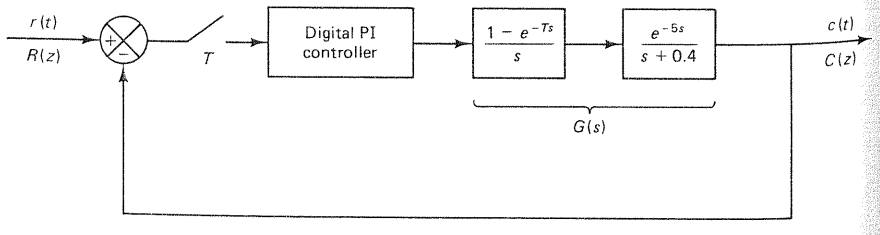

Figure 4–69 Digital control system for Problem B–4–11.

Problem B–4–12

Design a digital proportional-plus-derivative controller for the plant whose transfer function is $1/s^2$, as shown in Figure 4–70. It is desired that the damping ratio ζ of the dominant closed-loop poles be 0.5 and the undamped natural frequency be 4 rad/sec. The sampling period is 0.1 sec, or $T = 0.1$. After the controller is designed, determine the number of samples per cycle of damped sinusoidal oscillation.

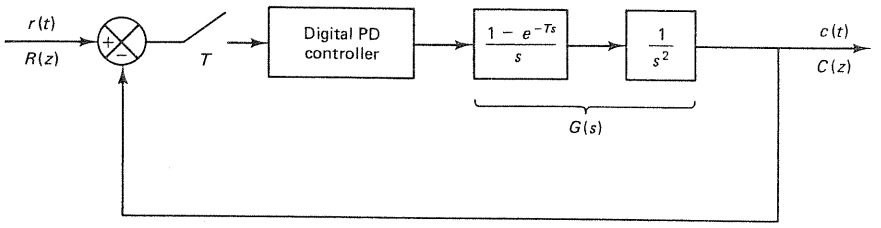

Figure 4–70 Digital control system for Problem B–4–12.

Problem B–4–13

Referring to the system considered in Problem A–4–9, redesign the digital controller so that the static velocity error constant K_v is 12 $\sec^{-1}$, without appreciably changing the locations of the dominant closed-loop poles in the z plane. The sampling period is assumed to be 0.2 sec, or $T = 0.2$. After the controller is redesigned, obtain the unit-step response and unit-ramp response of the digital control system.

Problem B–4–14

Consider the digital control system shown in Figure 4–71. Draw a Bode diagram in the w plane. Set the gain K so that the phase margin becomes equal to 50°. With the gain K so set, determine the gain margin and the static velocity error constant K_v. The sampling period is assumed to be 0.1 sec, or $T = 0.1$.

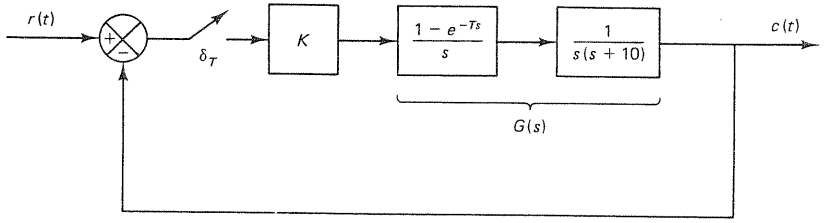

Figure 4–71 Digital control system for Problem B–4–14.

Problem B–4–15

Using the Bode diagram approach in the w plane, design a digital controller for the system shown in Figure 4–72. The design specifications are that the phase margin be 50°, the gain margin be at least 10 dB, and the static velocity error constant K_v be 20 $\sec^{-1}$. The sampling period is assumed to be 0.1 sec, or $T = 0.1$. After the controller is designed, calculate the number of samples per cycle of damped sinusoidal oscillation.

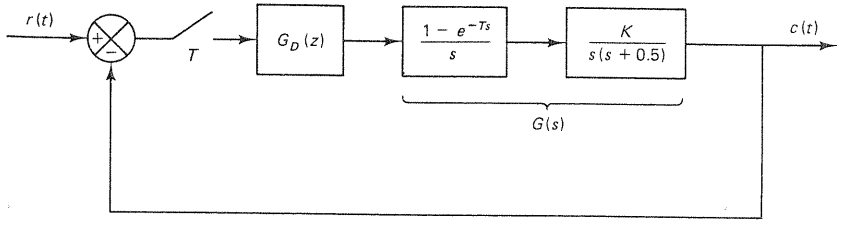

Figure 4–72 Digital control system for Problem B–4–15.

Problem B–4–16

Consider the digital control system shown in Figure 4–73. Using the Bode diagram approach in the w plane, design a digital controller such that the phase margin is 60°, the gain margin is 12 dB or more, and the static velocity error constant is 5 sec^{-1}. The sampling period is assumed to be 0.1 sec, or $T = 0.1$.

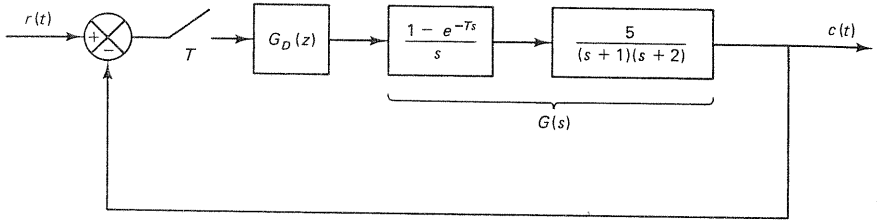

Figure 4–73 Digital control system for Problem B–4–16.

Problem B–4–17

Consider the system shown in Figure 4–74. Design a digital controller using a Bode diagram in the w plane such that the phase margin is 50° and the gain margin is at least 10 dB. It is desired that the static velocity error constant K_v be 10 sec^{-1}. The sampling period is specified as 0.1 sec, or $T = 0.1$. After the controller is designed, determine the number of samples per cycle of damped sinusoidal oscillation.

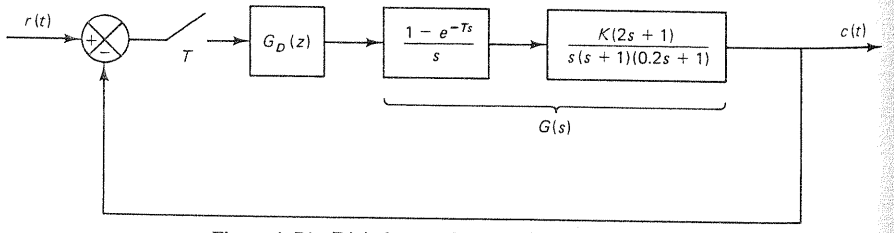

Figure 4–74 Digital control system for Problem B–4–17.

Problem B–4–18

Consider the digital control system shown in Figure 4–75. Design a digital controller $G_D(z)$ such that the system output will exhibit a deadbeat response to a unit step input (that is, the settling time will be the minimum possible and the steady-state error will be zero; also, the system output will not exhibit intersampling ripples after the settling time is reached). The sampling period T is assumed to be 1 sec, or $T = 1$.

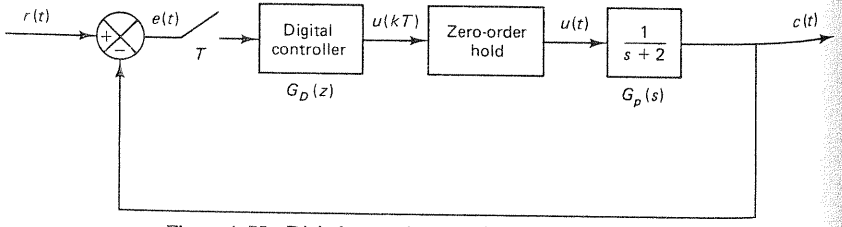

Figure 4–75 Digital control system for Problem B–4–18.

5

State-Space Analysis

5–1 INTRODUCTION

In Chapters 3 and 4 we were concerned with conventional methods for the analysis and design of control systems. Conventional methods such as the root-locus and frequency-response methods are useful for dealing with single-input–single-output systems. Conventional methods are conceptually simple and require only a reasonable number of computations, but they are applicable only to linear time-invariant systems having a single input and single output. They are based on the input–output relationship of the system, that is, the transfer function or the pulse transfer function. They do not apply to nonlinear systems except in simple cases. Also, the conventional methods do not apply to the design of optimal and adaptive control systems, which are mostly time varying and/or nonlinear.

A modern control system may have many inputs and many outputs, and these may be interrelated in a complicated manner. The state-space methods for the analysis and synthesis of control systems are best suited for dealing with multiple-input–multiple-output systems that are required to be optimal in some sense.

Concept of the State-Space Method. The state-space method is based on the description of system equations in terms of n first-order difference equations or differential equations, which may be combined into a first-order vector-matrix difference equation or differential equation. The use of the vector-matrix notation greatly simplifies the mathematical representation of the systems of equations.

System design by use of the state-space concept enables the engineer to design control systems with respect to given performance indexes. In addition, design in the state space can be carried out for a *class* of inputs, instead of a specific input