	Mnemonics	Operands	Description	Operation	Flags	#Clock	Note	
1	ADD	Rd, Rr	Add without Carry	Rd ← Rd + Rr	Z,C,N,V,S,H	1		Arithmetic and Logic Instructions
2	ADC	Rd, Rr	Add with Carry	Rd ← Rd + Rr + C	Z,C,N,V,S,H	1		
3	ADIW	Rd, K	Add Immediate to Word	Rd+1:Rd ← Rd+1:Rd + K	Z,C,N,V,S	2	(1)	
4	SUB	Rd, Rr	Subtract without Carry	Rd ← Rd -Rr	Z,C,N,V,S,H	1		
5	SUBI	Rd, K	Subtract Immediate	Rd ← Rd -K	Z,C,N,V,S,H	1		
6	SBC	Rd, Rr	Subtract with Carry	Rd ← Rd -Rr-C	Z,C,N,V,S,H	1		
7	SBCI	Rd, K	Subtract Immediate with Carry	Rd ← Rd -K -C	Z,C,N,V,S,H	1		
8	SBIW	Rd, K	Subtract Immediate from Word	Rd+1:Rd ← Rd+1:Rd -K	Z,C,N,V,S	2	(1)	
9	AND	Rd, Rr	Logical AND	Rd ← Rd • Rr	Z,N,V,S	1		
10	ANDI	Rd, K	Logical AND with Immediate	Rd ← Rd • K	Z,N,V,S	1		
11	OR	Rd, Rr	Logical OR	Rd ← Rd v Rr	Z,N,V,S	1		
12	ORI	Rd, K	Logical OR with Immediate	Rd ← Rd v K	Z,N,V,S	1		
13	EOR	Rd, Rr	Exclusive OR	Rd ← Rd ⊕ Rr	Z,N,V,S	1		
14	COM	Rd	One's Complement	Rd ← $FF -Rd	Z,C,N,V,S	1		
15	NEG	Rd	Two's Complement	Rd ← $00 -Rd	Z,C,N,V,S,H	1		
16	SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V,S	1		
17	CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FFh -K)	Z,N,V,S	1		
18	INC	Rd	Increment	Rd ← Rd + 1	Z,N,V,S	1		
19	DEC	Rd	Decrement	Rd ← Rd -1	Z,N,V,S	1		
20	TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V,S	1		
21	CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V,S	1		
22	SER	Rd	Set Register	Rd ← $FF	None	1		
23	MUL	Rd,Rr	Multiply Unsigned	R1:R0 ← Rd × Rr (UU)	Z,C	2	(1)	
24	MULS	Rd,Rr	Multiply Signed	R1:R0 ← Rd × Rr (SS)	Z,C	2	(1)	
25	MULSU	Rd,Rr	Multiply Signed with Unsigned	R1:R0 ← Rd × Rr (SU)	Z,C	2	(1)	
26	FMUL	Rd,Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd × Rr)<<1 (UU)	Z,C	2	(1)	
27	FMULS	Rd,Rr	Fractional Multiply Signed	R1:R0 ← (Rd × Rr)<<1 (SS)	Z,C	2	(1)	
28	FMULSU	Rd,Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd × Rr)<<1 (SU)	Z,C	2	(1)	
29	RJMP	k	Relative Jump	PC ← PC + k + 1	None	2		Branch Instructions
30	IJMP		Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	2	(1)	
31	EIJMP		Extended Indirect Jump to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	2	(1)	
32	JMP	k	Jump	PC ← k	None	3	(1)	
33	RCALL	k	Relative Call Subroutine	PC ← PC + k + 1	None	3 / 4	(4)	
34	ICALL		Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← 0	None	3 / 4	(1)(4)	
35	EICALL		Extended Indirect Call to (Z)	PC(15:0) ← Z, PC(21:16) ← EIND	None	4	(1)(4)	
36	CALL	k	Call Subroutine	PC ← k	None	4 / 5	(1)(4)	
37	RET		Subroutine Return	PC ← STACK	None	4 / 5	(4)	
38	RETI		Interrupt Return	PC ← STACK	I	4 / 5	(4)	
39	CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3		
40	CP	Rd,Rr	Compare	Rd -Rr	Z,C,N,V,S,H	1		
41	CPC	Rd,Rr	Compare with Carry	Rd -Rr -C	Z,C,N,V,S,H	1		
42	CPI	Rd,K	Compare with Immediate	Rd -K	Z,C,N,V,S,H	1		
43	SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3		
44	SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3		
45	SBIC	A, b	Skip if Bit in I/O Register Cleared	if(I/O(A,b)=0) PC ← PC + 2 or 3	None	1 / 2 / 3		
46	SBIS	A, b	Skip if Bit in I/O Register Set	If(I/O(A,b)=1) PC ← PC + 2 or 3	None	1 / 2 / 3		
47	BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ←PC+k + 1	None	1 / 2		
48	BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ←PC+k + 1	None	1 / 2		
49	BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2		
50	BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2		
51	BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC +k +1	None	1/ 2		
52	BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC +k +1	None	1/ 2		
53	BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC +k +1	None	1/ 2		
54	BRLO	k	Branch if Lower	if (C = 1) then PC ← PC +k +1	None	1/ 2		
55	BRMI	k	Branch if Minus	if (N = 1) then PC ← PC +k +1	None	1/ 2		
56	BRPL	k	Branch if Plus	if (N = 0) then PC ← PC +k +1	None	1/ 2		
57	BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2		
58	BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2		
59	BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC +k +1	None	1/ 2		
60	BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC +k +1	None	1/ 2		
61	BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2		
62	BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2		
63	BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC +k +1	None	1/ 2		
64	BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC +k +1	None	1/ 2		
65	BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2		
66	BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2		
67	BREAK		Break	(See specific descr. for BREAK)	None	1	(1)	MCU Control Instructions
68	NOP		No Operation		None	1		
69	SLEEP		Sleep	(see specific descr. for Sleep)	None	1		
70	WDR		Watchdog Reset	(see specific descr. for WDR)	None	1		

	Mnemonics	Operands	Description	Operation	Flags	#Clock Note	
71	MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1	Data Transfer Instructions
72	MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1 (1)	
73	LDI	Rd, K	Load Immediate	Rd ← K	None	1	
74	LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2 (1)(4)	
75	LD	Rd, X	Load Indirect	Rd ← (X)	None	2 (2)(4)	
76	LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X), X ← X + 1	None	2 (2)(4)	
77	LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X-1, Rd ← (X)	None	2 (2)(4)	
78	LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2 (2)(4)	
79	LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y), Y ← Y + 1	None	2 (2)(4)	
80	LD	Rd, -Y	Load Indirect and Pre-Decrement	Y ← Y-1, Rd ← (Y)	None	2 (2)(4)	
81	LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2 (1)(4)	
82	LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2 (2)(4)	
83	LD	Rd, Z+	Load Indirect and Post-Increment	Rd ← (Z), Z ← Z+1	None	2 (2)(4)	
84	LD	Rd, -Z	Load Indirect and Pre-Decrement	Z ← Z-1, Rd ← (Z)	None	2 (2)(4)	
85	LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z+q)	None	2 (1)(4)	
86	STS	k, Rr	Store Direct to data space	(k) ← Rd	None	2 (1)(4)	
87	ST	X, Rr	Store Indirect	(X) ← Rr	None	2 (2)(4)	
88	ST	X+, Rr	Store Indirect and Post-Increment	(X) ← Rr, X ← X + 1	None	2 (2)(4)	
89	ST	-X, Rr	Store Indirect and Pre-Decrement	X ← X-1, (X) ← Rr	None	2 (2)(4)	
90	ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2 (2)(4)	
91	ST	Y+, Rr	Store Indirect and Post-Increment	(Y) ← Rr, Y ← Y + 1	None	2 (2)(4)	
92	ST	-Y, Rr	Store Indirect and Pre-Decrement	Y ← Y-1, (Y) ← Rr	None	2 (2)(4)	
93	STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2 (1)(4)	
94	ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2 (2)(4)	
95	ST	Z+, Rr	Store Indirect and Post-Increment	(Z) ← Rr, Z ← Z + 1	None	2 (2)(4)	
96	ST	-Z, Rr	Store Indirect and Pre-Decrement	Z ← Z-1, (Z) ← Rr	None	2 (2)(4)	
97	STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2 (1)(4)	
98	LPM		Load Program Memory	R0 ← (Z)	None	3 (3)	
99	LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3 (3)	
100	LPM	Rd, Z+	Load Program Memory and Post-Incremer	Rd ← (Z), Z ← Z+1	None	3 (3)	
101	ELPM		Extended Load Program Memory	R0 ← (RAMPZ:Z)	None	3 (1)	
102	ELPM	Rd, Z	Extended Load Program Memory	Rd ← (RAMPZ:Z)	None	3 (1)	
103	ELPM	Rd, Z+	Extended Load Program Memory and Post	Rd ← (RAMPZ:Z), Z ← Z + 1	None	3 (1)	
104	SPM		Store Program Memory	(Z) ← R1:R0	None	-(1)	
105	IN	Rd, A	In From I/O Location	Rd ← I/O(A)	None	1	
106	OUT	A, Rr	Out To I/O Location	I/O(A) ← Rr	None	1	
107	PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2 (1)	
108	POP	Rd	Pop Register from Stack	Rd ← STACK	None	2 (1)	
109	LSL	Rd	Logical Shift Left	Rd(n+1)←Rd(n),Rd(0)←0,C←Rd(7)	Z,C,N,V,H	1	Bit and Bit-test Instructions
110	LSR	Rd	Logical Shift Right	Rd(n)←Rd(n+1),Rd(7)←0,C←Rd(0)	Z,C,N,V	1	
111	ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)←Rd(n),C←Rd(7)	Z,C,N,V,H	1	
112	ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)←Rd(n+1),C←Rd(0)	Z,C,N,V	1	
113	ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1	
114	SWAP	Rd	Swap Nibbles	Rd(3..0) ↔ Rd(7..4)	None	1	
115	BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1	
116	BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1	
117	SBI	A, b	Set Bit in I/O Register	I/O(A, b) ← 1	None	2	
118	CBI	A, b	Clear Bit in I/O Register	I/O(A, b) ← 0	None	2	
119	BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1	
120	BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1	
121	SEC		Set Carry	C ← 1	C	1	
122	CLC		Clear Carry	C ← 0	C	1	
123	SEN		Set Negative Flag	N ← 1	N	1	
124	CLN		Clear Negative Flag	N ← 0	N	1	
125	SEZ		Set Zero Flag	Z ← 1	Z	1	
126	CLZ		Clear Zero Flag	Z ← 0	Z	1	
127	SEI		Global Interrupt Enable	I ← 1	I	1	
128	CLI		Global Interrupt Disable	I ← 0	I	1	
129	SES		Set Signed Test Flag	S ← 1	S	1	
130	CLS		Clear Signed Test Flag	S ← 0	S	1	
131	SEV		Set Two's Complement Overflow	V ← 1	V	1	
132	CLV		Clear Two's Complement Overflow	V ← 0	V	1	
133	SET		Set T in SREG	T ← 1	T	1	
134	CLT		Clear T in SREG	T ← 0	T	1	
135	SEH		Set Half Carry Flag in SREG	H ← 1	H	1	
136	CLH		Clear Half Carry Flag in SREG	H ← 0	H	1	
137							
138							